CLAIMS

1. A process for manufacturing a semiconductor device, comprising the steps of:

forming a lower gate electrode film on a semiconductor substrate via a gate insulating film;

forming an upper gate electrode film on the lower gate electrode film, the upper gate electrode film being made of a material having a lower oxidation rate than that of the lower gate electrode film;

forming a gate electrode by patterning the upper gate electrode film and the lower gate electrode film, the gate electrode comprising a lower gate electrode element and an upper gate electrode element;

forming source/drain regions by introducing an impurity into the semiconductor substrate; and

forming oxide film sidewalls by oxidizing the side faces of the lower gate electrode element and the upper gate electrode element, the thickness of the oxide film sidewalls in the gate length direction being larger at the sides of the lower gate electrode element than at the sides of the upper gate electrode element.

2. A process for manufacturing the semiconductor device according to claim 1, wherein the gate length of

the lower gate electrode element is made shorter than that of the upper gate electrode element by the step of forming the oxide film sidewalls.

3. A process for manufacturing the semiconductor device according to claim 1, wherein the lower gate electrode film is formed of a Group IV semiconductor.

4. A process for manufacturing the semiconductor device according to claim 3, wherein the lower gate electrode film contains SiGe.

5. A process for manufacturing the semiconductor device according to claim 4, wherein the composition ratio of Ge is not less than 0.05 and not more than 0.90.

6. A process for manufacturing the semiconductor device according to claim 4, wherein the lower gate electrode film contains C.

7. A process for manufacturing the semiconductor device according to claim 3, wherein the upper gate electrode element is composed of Si.

8. A process for manufacturing the semiconductor

device according to claim 4, wherein the upper gate electrode film is formed of a Group IV semiconductor containing SiGe, and wherein the upper gate electrode film has a lower Ge composition ratio than that of the lower gate electrode film.

9. A process for manufacturing the semiconductor device according to claim 4, wherein the step of forming the oxide film sidewalls is performed by oxidizing the lower gate electrode element to thereby form a region in both side portions of the lower gate electrode element in the gate length direction, the regions having a higher Ge composition ratio than that of the central portion of the lower gate electrode element.

10. A process for manufacturing the semiconductor device according to claim 1, wherein the step of forming the oxide film sidewalls is performed under an atmosphere containing water vapor.

11. A process for manufacturing the semiconductor device according to claim 4, wherein the semiconductor substrate includes a channel region containing SiGe or SiGeC between the source/drain regions.

12. A process for manufacturing the semiconductor device according to claim 4, wherein the step of forming the lower gate electrode element is performed by forming a first region and second regions, the second regions sandwiching the first region therebetween in the gate length direction and having a higher Ge composition ratio than that of the first region, and wherein the step of forming the gate electrode is performed by patterning the lower gate electrode film and the upper gate electrode film such that the second regions are located in both side portions of the lower gate electrode element in the gate length direction.

13. A semiconductor device comprising:

a semiconductor substrate;

a lower gate electrode element formed on the semiconductor substrate via a gate insulating film;

an upper gate electrode element formed on the lower gate electrode element and made of a material having a lower oxidation rate than that of the lower gate electrode element;

source/drain regions formed in the semiconductor substrate below the lower gate electrode element in such a manner as to sandwich a channel region; and

oxide film sidewalls formed by oxidizing the side faces

of the lower gate electrode element and the upper gate electrode element, the thickness of the oxide film sidewalls in the gate length direction being larger at the sides of the lower gate electrode element than at the sides of the upper gate electrode element.

14. A semiconductor device according to claim 13, wherein the gate length of the lower gate electrode element is shorter than that of the upper gate electrode element.

15. A semiconductor device according to claim 13, wherein the lower gate electrode element is formed of a Group IV semiconductor.

16. A semiconductor device according to claim 15, wherein the lower gate electrode element contains SiGe.

17. A semiconductor device according to claim 16, wherein the composition ratio of Ge is not less than 0.05 and not more than 0.90.

18. A semiconductor device according to claim 16, wherein the lower gate electrode element contains C.

19. A semiconductor device according to claim 16, wherein the upper gate electrode element is composed of Si.

20. A semiconductor device according to claim 16, wherein the lower gate electrode element includes regions in both side portions thereof in the gate length direction, the regions having a higher Ge composition ratio than that of the central portion of the lower gate electrode element.

21. A semiconductor device according to claim 16, wherein the semiconductor substrate includes the channel region containing SiGe or SiGeC between the source/drain regions.